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DATE: Tuesday, April 19, 2005

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,JPAB; PLUR=YES; OP=OR	
☐	L14	L13 and simulation	17
☐	L13	l5 and L12	24
☐	L12	linear same network	20777
☐	L11	L10 and (communication same network)	1
☐	L10	L9 and telecommunication	1
☐	L9	L8 and network	18
☐	L8	L5 and simulation and (netlist or net)	19
☐	L7	L5 and simulation and (netlist or net) and (diagonal$ or chain$)	11
☐	L6	L5 and simulation and (netlist or net) and (diagonal$)	11
☐	L5	parameter same (admittance or conductance) same matri$	100
☐	L4	L3 and parameter and chain$4	4
☐	L3	simulation and netlist and circuit and admittance	20
☐	L2	krakovian and admittance	1
☐	L1	krakovian and matrix and admittance	1

END OF SEARCH HISTORY

US006785873B1

(12) **United States Patent**
Tseng

(10) **Patent No.: US 6,785,873 B1**
(45) **Date of Patent: Aug. 31, 2004**

(54) **EMULATION SYSTEM WITH MULTIPLE ASYNCHRONOUS CLOCKS**

(75) Inventor: **Ping-Sheng Tseng**, Sunnyvale, CA (US)

(73) Assignee: **Axis Systems, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 761 days.

(21) Appl. No.: **09/591,683**

(22) Filed: **Jun. 9, 2000**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/546,554, filed on Apr. 10, 2000, which is a continuation-in-part of application No. 09/373,014, filed on Aug. 11, 1999, which is a continuation-in-part of application No. 09/144,222, filed on Aug. 31, 1999, now Pat. No. 6,321,366, which is a continuation-in-part of application No. 08/850,136, filed on May 2, 1997, now Pat. No. 6,009,256.

(51) **Int. Cl.**[7] **G06F 17/50**

(52) **U.S. Cl.** **716/4**; 716/1

(58) **Field of Search** 716/4, 1, 5, 6

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,836,889	A *	9/1974	Kotok et al.	710/264
4,144,448	A *	3/1979	Pisciotta et al.	714/814
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5,126,950	A *	6/1992	Rees et al.	716/4
5,425,036	A *	6/1995	Liu et al.	714/735
5,596,742	A *	1/1997	Agarwal et al.	716/16
6,084,930	A *	7/2000	Dinteman	375/354
6,204,711	B1 *	3/2001	Scarlett et al.	327/291

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O'Leary et al., "Synchronous Emulation of Asynchronous Circuits", Feb. 1997, IEEE Transactions on Computer–Aided Design o Integrated Circuit and System, vol. 16, iss. 2, pp. 205–209.*

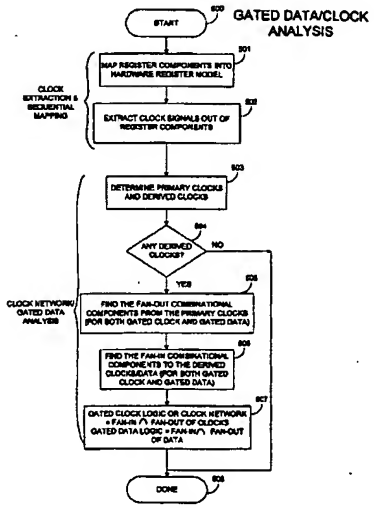
* cited by examiner

Primary Examiner—Matthew Smith
Assistant Examiner—Sun James Lin
(74) *Attorney, Agent, or Firm*—Burns, Doane, Swecker & Mathis LLP

(57) **ABSTRACT**

An emulation system includes a clock generation logic for generating multiple asynchronous clocks, where each generated clock's relative phase relationship with respect to all other generated clocks is strictly controlled to speed up the emulation logic evaluation. Unlike statically designed emulator systems known in the prior art, the speed of the logic evaluation in the emulator need not be slowed down to the worst possible evaluation time since the clocking is generated internally in the emulator and carefully controlled. The emulation system does not concern itself with the absolute time duration of each clock, because only the phase relationship among the multiple asynchronous clocks is important. By retaining the phase relationship (and the initial values) among the multiple asynchronous clocks, the speed of the logic evaluation in the emulator can be increased. The RCC clock generation logic comprises a clock generation scheduler and a set of clock generation slices, where each clock generation slice generates a clock. The clock generation scheduler compares each clock's next toggle point from the current time, toggles the clock associated with the winning next toggle point, determines the new current time, updates the next toggle point information for all of the clock generation slices, and performs the comparison again in the next evaluation cycle. In the update phase, the winning slice updates its register with a new next toggle point, while the losing slices merely updates their respective registers by adjusting for the new current time.

20 Claims, 99 Drawing Sheets



US005384710A

United States Patent [19]

Lam et al.

[11] Patent Number: 5,384,710

[45] Date of Patent: Jan. 24, 1995

[54] CIRCUIT LEVEL NETLIST GENERATION

[75] Inventors: Nim C. Lam, Sunnyvale; Amrit K. Lalchandani, Mountain View, both of Calif.

[73] Assignee: National Semiconductor Corporation, Santa Clara, Calif.

[21] Appl. No.: 173,808

[22] Filed: Dec. 22, 1993

Related U.S. Application Data

[63] Continuation of Ser. No. 493,057, Mar. 13, 1990, abandoned.

[51] Int. Cl.[6] G06F 15/60

[52] U.S. Cl. 364/489; 364/488

[58] Field of Search 364/488, 489, 490, 491

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"Hierarchical Functional Verification for Cell-Based Design Styles" by Chen et al., IEE Proceedings, vol. 134, Part G, No. 2, Apr. 1987, pp. 103–109.

"Programs for Verifying Circuit Connectivity of MOS/LSI Mask Artwork" by Takashima et al., IEEE 19th Design Automation Conf., 1982, pp. 544–550.

Primary Examiner—Vincent N. Trans

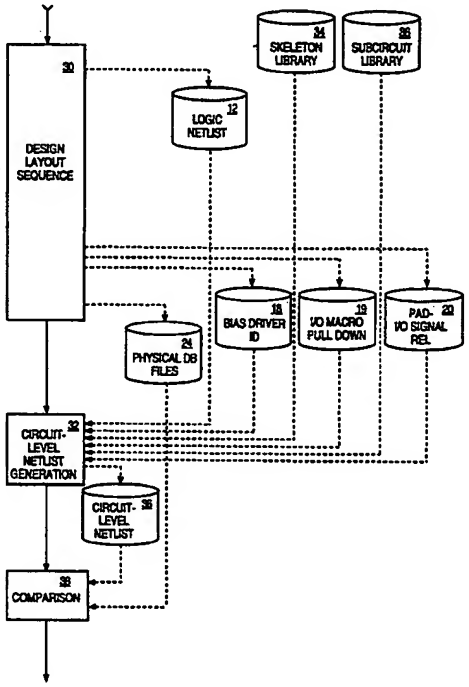
Attorney, Agent, or Firm—H. Donald Nelson; David H. Carroll; Stephen R. Robinson

[57] ABSTRACT

A design layout sequence for an application specific integrated circuit such as a gate array includes a schematic capture step, which results in a logic netlist file, and a placement and routing step which results in a number of various files defining, for example, bias drivers, I/O macros, and relationships between chip pads and I/O signals. The design layout sequence culminates in a physical data base file. The connectivity of this physical data base file is checked by first generating a circuit level netlist file for the entire option, and then comparing the circuit level netlist with the physical data base file. In generating the circuit level netlist file, information is obtained from the logic netlist file, as well as from some of the other files created in the design-layout sequence. In addition, basic information from which the circuit level netlist is constructed is obtained from a skeleton file library and a subcircuit library. The contents and methodology for deriving the skeleton file library and the subcircuit library are discussed.

11 Claims, 53 Drawing Sheets

Microfiche Appendix Included
(483 Microfiche, 6 Pages)



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Search Results - Record(s) 1 through 11 of 11 returned.

☐ 1. Document ID: US 20050027491 A1

Using default format because multiple data bases are involved.

L6: Entry 1 of 11 File: PGPB Feb 3, 2005

PGPUB-DOCUMENT-NUMBER: 20050027491
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050027491 A1

TITLE: Symbolic analysis of electrical circuits for application in telecommunications

PUBLICATION-DATE: February 3, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Fertner, Antoni	Solna		SE	
Luppert, Edwin	Sodertalje		SE	

US-CL-CURRENT: 702/196

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6577992 B1

L6: Entry 2 of 11 File: USPT Jun 10, 2003

US-PAT-NO: 6577992
DOCUMENT-IDENTIFIER: US 6577992 B1

TITLE: Transistor level circuit simulator using hierarchical data

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 3. Document ID: US 6563150 B1

L6: Entry 3 of 11 File: USPT May 13, 2003

US-PAT-NO: 6563150
DOCUMENT-IDENTIFIER: US 6563150 B1

TITLE: High frequency field effect transistor

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 4. Document ID: US 6134513 A

L6: Entry 4 of 11 File: USPT Oct 17, 2000

US-PAT-NO: 6134513
DOCUMENT-IDENTIFIER: US 6134513 A

TITLE: Method and apparatus for simulating large, hierarchical microelectronic resistor circuits

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 5. Document ID: US 5861644 A

L6: Entry 5 of 11 File: USPT Jan 19, 1999

US-PAT-NO: 5861644
DOCUMENT-IDENTIFIER: US 5861644 A

TITLE: High-frequency traveling wave field-effect transistor

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 6. Document ID: US 5627389 A

L6: Entry 6 of 11 File: USPT May 6, 1997

US-PAT-NO: 5627389
DOCUMENT-IDENTIFIER: US 5627389 A
** See image for Certificate of Correction **

TITLE: High-frequency traveling wave field-effect transistor

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 7. Document ID: US 5502392 A

L6: Entry 7 of 11 File: USPT Mar 26, 1996

US-PAT-NO: 5502392
DOCUMENT-IDENTIFIER: US 5502392 A

TITLE: Methods for the measurement of the frequency dependent complex propagation matrix, impedance matrix and admittance matrix of coupled transmission lines

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 8. Document ID: US 5467291 A

L6: Entry 8 of 11 File: USPT Nov 14, 1995

US-PAT-NO: 5467291
DOCUMENT-IDENTIFIER: US 5467291 A

TITLE: Measurement-based system for modeling and simulation of active semiconductor devices over an extended operating frequency range

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 9. Document ID: US 5394346 A

L6: Entry 9 of 11 File: USPT Feb 28, 1995

US-PAT-NO: 5394346
DOCUMENT-IDENTIFIER: US 5394346 A

TITLE: Simulation of an electronic system including analog and digital circuitry using high level macro models

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 10. Document ID: US 5313398 A

L6: Entry 10 of 11 File: USPT May 17, 1994

US-PAT-NO: 5313398
DOCUMENT-IDENTIFIER: US 5313398 A

TITLE: Method and apparatus for simulating a microelectronic circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 11. Document ID: US 4677386 A

L6: Entry 11 of 11 File: USPT Jun 30, 1987

US-PAT-NO: 4677386
DOCUMENT-IDENTIFIER: US 4677386 A
** See image for Certificate of Correction **

TITLE: Method of interpreting impedance distribution of an earth formation obtained by a moving array using end emitting current electrodes sequentially activated and a series of potential electrodes

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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Search Results - Record(s) 1 through 15 of 24 returned.

☐ 1. Document ID: US 20050049838 A1

Using default format because multiple data bases are involved.

L13: Entry 1 of 24 File: PGPB Mar 3, 2005

PGPUB-DOCUMENT-NUMBER: 20050049838
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050049838 A1

TITLE: Multiphase physical transport modeling method and modeling system

PUBLICATION-DATE: March 3, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Danko, George	Reno	NV	US	

US-CL-CURRENT: 703/2

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20050027491 A1

L13: Entry 2 of 24 File: PGPB Feb 3, 2005

PGPUB-DOCUMENT-NUMBER: 20050027491
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050027491 A1

TITLE: Symbolic analysis of electrical circuits for application in telecommunications

PUBLICATION-DATE: February 3, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Fertner, Antoni	Solna		SE	
Luppert, Edwin	Sodertalje		SE	

US-CL-CURRENT: 702/196

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 20040031001 A1

L13: Entry 3 of 24 File: PGPB Feb 12, 2004

PGPUB-DOCUMENT-NUMBER: 20040031001
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040031001 A1

TITLE: MOSFET modeling for IC design accurate for high frequencies

PUBLICATION-DATE: February 12, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Zhang, Xisheng	Sunnyvale	CA	US	
Liang, Hancheng	San Jose	CA	US	
Liu, Zhihong	Cupertino	CA	US	
Guo, Jianhe	Santa Clara	CA	US	

US-CL-CURRENT: 716/4; 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 20030200039 A1

L13: Entry 4 of 24 File: PGPB Oct 23, 2003

PGPUB-DOCUMENT-NUMBER: 20030200039
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030200039 A1

TITLE: Method, apparatus, and article of manufacture for predicting electrical behavior of a multiport device having balanced device ports

PUBLICATION-DATE: October 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Adamian, Vahe?apos; A.	Lexington	MA	US	
Cole, J. Bradford	Westford	MA	US	

US-CL-CURRENT: 702/65

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 5. Document ID: US 20020183990 A1

L13: Entry 5 of 24 File: PGPB Dec 5, 2002

PGPUB-DOCUMENT-NUMBER: 20020183990
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020183990 A1

TITLE: Circuit simulation

PUBLICATION-DATE: December 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wasynczuk, Oleg	West Lafayette	IN	US	
Jatskevich, Juri V.	Lafayette	IN	US	

US-CL-CURRENT: 703/2

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 6. Document ID: US 20010029601 A1

L13: Entry 6 of 24 File: PGPB Oct 11, 2001

PGPUB-DOCUMENT-NUMBER: 20010029601
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010029601 A1

TITLE: Semiconductor device analyzer, method for analyzing/manufacturing semiconductor device, and storage medium storing program for analyzing semiconductor device

PUBLICATION-DATE: October 11, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kimura, Tomohisa	Tokyo		JP	
Okumura, Makiko	Kanagawa		JP	

US-CL-CURRENT: 716/19; 716/4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 7. Document ID: US 6851097 B2

L13: Entry 7 of 24 File: USPT Feb 1, 2005

US-PAT-NO: 6851097
DOCUMENT-IDENTIFIER: US 6851097 B2

TITLE: MOSFET modeling for IC design accurate for high frequencies

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 8. Document ID: US 6785625 B1

L13: Entry 8 of 24 File: USPT Aug 31, 2004

US-PAT-NO: 6785625
DOCUMENT-IDENTIFIER: US 6785625 B1

TITLE: Characterizing multi-port cascaded networks

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 9. Document ID: US 6757625 B2

L13: Entry 9 of 24 File: USPT Jun 29, 2004

US-PAT-NO: 6757625
DOCUMENT-IDENTIFIER: US 6757625 B2

TITLE: Method, apparatus, and article of manufacture for predicting electrical behavior of a multiport device having balanced device ports

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 10. Document ID: US 6618837 B1

L13: Entry 10 of 24 File: USPT Sep 9, 2003

US-PAT-NO: 6618837
DOCUMENT-IDENTIFIER: US 6618837 B1
** See image for Certificate of Correction **

TITLE: MOSFET modeling for IC design accurate for high frequencies

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 11. Document ID: US 6563150 B1

L13: Entry 11 of 24 File: USPT May 13, 2003

US-PAT-NO: 6563150
DOCUMENT-IDENTIFIER: US 6563150 B1

TITLE: High frequency field effect transistor

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 12. Document ID: US 6202041 B1

L13: Entry 12 of 24 File: USPT Mar 13, 2001

US-PAT-NO: 6202041
DOCUMENT-IDENTIFIER: US 6202041 B1

TITLE: Electrical power network modelling method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 13. Document ID: US 5946482 A

L13: Entry 13 of 24 File: USPT Aug 31, 1999

US-PAT-NO: 5946482
DOCUMENT-IDENTIFIER: US 5946482 A

TITLE: Method and apparatus for using parameters to simulate an electronic circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 14. Document ID: US 5781764 A

L13: Entry 14 of 24 File: USPT Jul 14, 1998

US-PAT-NO: 5781764
DOCUMENT-IDENTIFIER: US 5781764 A
** See image for Certificate of Correction **

TITLE: Method and apparatus for generation a system component model and for evaluation system parameters in relation to such model

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 15. Document ID: US 5777475 A

L13: Entry 15 of 24 File: USPT Jul 7, 1998

US-PAT-NO: 5777475
DOCUMENT-IDENTIFIER: US 5777475 A

TITLE: Automatic impedance adapter for a H.F. emitter or receiver in a nuclear spin tomography installation and process for operating the device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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Terms	Documents
L5 and L12	24
